Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID K. VAVRO and JAMES A. MITCHELL

Appeal No. 2003-1635
Application No. 09/465,634

ON BRIEF

Before FLEMING, DIXON, and GROSS, ***Administrative Patent Judges***.
GROSS, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 24, which are all of the claims pending in this application.

Appellants' invention relates to a digital signal processor with several individual processors including a master processor which controls the other processors. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A digital signal processor comprising:

a mathematical processor;

an input processor that processes input signals to the digital signal processor;

an output processor that processes output signals from the digital signal processor;

a master processor that controls said mathematical processor, said input processor and said output processor; and

a storage selectively accessible by each of said processors.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Nakagawa et al. (Nakagawa)	5,241,679	Aug. 31, 1993
Whittaker et al. (Whittaker)	5,968,167	Oct. 19, 1999
Kitamura	EP0942603	Sep. 15, 1999

Claim 15 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 1 through 4, 6, 8, 9, 15 through 17, 23, and 24 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Kitamura.

Claims 5, 7, 14, and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kitamura.

Claim 10 stands rejected under 35 U.S.C. § 103 as being unpatentable over Kitamura in view of Whittaker.

Claims 11 through 13 and 18 through 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kitamura in view of Nakagawa.

Reference is made to the Examiner's Answer (Paper No. 11, mailed February 11, 2002) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 10, filed January 22, 2003) for appellants' arguments thereagainst.

OPINION

As a preliminary matter, we note that appellants indicate on page 15 of the Brief that claims 1 through 15 are to be grouped together, but separately from claims 16 through 24, which are also to be grouped together. However, the argument presented for claim 16 (Brief, page 17) is identical to the argument presented for claim 1 (Brief, pages 16-17). Therefore, appellants have failed to present separate arguments in accordance with 37 C.F.R. § 1.192(c)(7) (which was in effect at the time of the Brief). Accordingly, we shall group claim 16 and its dependents with claim 1 and its dependents.

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the indefiniteness rejection of claim 15. In addition, we will affirm the anticipation rejection of claims 1

through 4, 6, 8, 9, 15 through 17, 23, and 24 and the obviousness rejections of claims 5, 7, 10 through 14, and 18 through 22.

Regarding the rejection of claim 15 under 35 U.S.C. § 112, second paragraph, the examiner asserts (Answer, page 11) that there are two ways to interpret "multi-cycled mathematical processor." The examiner directs our attention to appellants' specification, page 24, lines 20-23, as support for one interpretation, that "the processor requires multiple cycles to complete an operation," and to page 23, line 19, for the other interpretation, that "it is operated at various cycle speeds." Although we agree with the examiner's interpretation of the page 24 excerpt, we disagree with the interpretation of the page 23 excerpt. The portion referenced on page 23 also suggests that the processor requires multiple cycles, though they may also be at different speeds due to the "self-timed" aspect. Accordingly, we find claim 15 to be definite, and we will reverse the rejection under 35 U.S.C. § 112, second paragraph.

As to the anticipation rejection of claims 1 through 4, 6, 8, 9, 15 through 17, 23, and 24, appellants' sole argument (Brief, pages 16-17) is that Kitamura fails to disclose a mathematical processor. Appellants assert (Brief, page 16) that data processing unit 5 (the element the examiner gave as a

mathematical processor (Answer, page 4)) splices video data, and "[t]here is no indication that this device can be considered to be a mathematical processor."

The examiner explains (Answer, pages 12-13) that data processing unit 5 acts upon encoded video data DA and DB, "which are combinations of bits, or numbers." The examiner contends that acting upon bits or numbers constitutes mathematical operations. Further, the examiner asserts that the blanking generator 20, which is part of processing unit 5, sets a differential value between two macroblocks, and thereby performs subtraction, a mathematical operation. Accordingly, the examiner concludes that data processing unit 5 is a mathematical processor.

Appellants do not provide a definition of a mathematical processor in the specification. Instead, appellants (page 5, lines 17-23) provide examples of mathematical processors including add and subtract and multiply and accumulate processors. Appellants add that other mathematical processors may be used based on the particular needs in particular applications. Thus, appellants suggest that there are other types of mathematical processors and that the invention is not limited to the examples given in the specification.

We find that the examiner clearly explained how Kitamura's processor 5 does mathematical functions. In addition, Figure 20 further shows how the operations of the blanking generator are mathematical functions. Therefore, we agree with the examiner that since processor 5 acts on bits or numbers, and since the blanking generator is part of processor 5 and performs mathematical operations, processor 5 is a mathematical processor. Consequently, we will sustain the anticipation rejection of claims 1 through 4, 6, 8, 9, 15 through 17, 23, and 24.

Appellants presented no further arguments for the obviousness rejection of claims 5, 7, 14, and 22 over Kitamura alone, nor for the addition of Whittaker for the rejection of claim 10, nor for the addition of Nakagawa for the rejection of claims 11 through 13 and 18 through 21. Therefore, we will affirm the rejections of claims 5, 7, 10 through 14 and 18 through 22 for substantially the same reasons as explained ***supra***.

CONCLUSION

The decision of the examiner rejecting claim 15 under 35 U.S.C. § 112, second paragraph is reversed. The decision of the examiner rejecting claims 1 through 4, 6, 8, 9, 15 through

17, 23, and 24 under 35 U.S.C. § 102(a) and claims 5, 7, 10 through 14, and 18 through 22 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

MICHAEL R. FLEMING)
Administrative Patent Judge)
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JOSEPH L. DIXON) BOARD OF PATENT
Administrative Patent Judge) APPEALS
) AND
) INTERFERENCES
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ANITA PELLMAN GROSS)
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